## **CLAIMS**

What is claimed is:

- 1. A mathematical engine comprising:
- a parallel output shift register receiving data to be processed; and a processor, including an adder tree using a plurality of arithmetic logic unit (ALU) circuits, for accepting the output of the shift register and for providing a data output; whereby the shift register includes a selectable initial position, to selectively output the data based upon the capacity of the processor.
- 2. The mathematical engine of claim 1, further comprising a multiplexer, for receiving an output from the parallel output shift register and providing data from the parallel output shift register to the processor.
- 3. The mathematical engine of claim 2 comprising at least one enable circuit, to selectively enable the output from the shift register.
- 4. The mathematical engine of claim 1, wherein said data includes both real and imaginary components.
- 5. A calculation unit for performing a plurality of different types of calculations, the calculation unit comprising:
  - a parallel output shift register;
- a multiplexer, for receiving the output from said shift register and providing an output to an adder tree;
- the adder tree comprising a plurality of arithmetic logic units (ALUs); and
- a selection circuit for selectively enabling the shift register and the multiplexer to apply certain portions of the input data to the adder tree, to perform different calculations.

7

- 6. The calculation unit of claim 5, further comprising, at least one selectable memory having a data width of at least a multiple of a data width of the adder tree.
- 7. A mathematical engine for performing calculations, the mathematical engine including:

at least one input memory for storing input data;

a selectable memory for receiving the input data from said at least one input memory and for providing a selectable output via a plurality of folds, wherein each fold comprises at least one position within the selectable memory; and

a processor array having a plurality of processors for receiving an output from the selectable memory and selectively providing an output.

- 8. The mathematical engine of claim 7, further comprising an enablement circuit to selectively control said at least one input memory and said selectable memory depending upon the desired mathematical calculation.
- 9. The mathematical engine of claim 8, further including an adder tree, having a plurality of arithmetic logic unit circuits, for receiving an output from the processor array and for processing the output; and

an accumulation circuit for receiving and accumulating each output from the adder tree;

whereby said enablement circuit further controls at least a portion of the adder tree, support the desired mathematical calculation.

10. A computation circuit for resolving complex functions; the computation circuit comprising:

a memory, for receiving input data for complex resolution; a store, for storing an operational factor for the complex function;

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a multiplexer, for receiving an input from the memory and the operational factor;

a processing array circuit, for processing according to a number of bit locations stored by the memory, the processing array circuit including an output from the multiplexer and at least some of the input data;

a complex adder tree receiving outputs from the processing array and providing an added output; and

an accumulator circuit receiving an output from the adder tree and providing an accumulated complex output.

- 11. The computation circuit of claim 10 wherein the memory includes a parallel output shift register having includes a selectable initial position.
- 12. The computation circuit of claim 10, further comprising providing a twiddle factor as the operational factor, for performing discrete Fourier transforms (DFTs), wherein the multiplexer receives its input from the memory and the operational factor.
  - 13. A computation circuit for resolving complex functions, comprising: a memory, for receiving complex input data for resolution; a store for a twiddle factor;

a multiplexer, for receiving the complex input data from the memory and the twiddle factor from the store;

a processing array circuit, for processing data according to a number of bit locations stored by the memory, the processing array circuit including an output from the multiplexer and at least some of the input data;

a complex adder tree receiving outputs from the processing array and providing an added output; and

an accumulator for accounting said added outputs.

- 14. The computation circuit of claim 13 wherein the memory includes a parallel output shift register includes a selectable initial position.
- 15. A method for electronically resolving complex functions, the method comprising:

providing input data for complex resolution from a first memory; providing an operational factor for the complex function from a second memory, and multiplexing the operational factor with data from the first memory to provide multiplexed data; and

supplying a select portion of the multiplexed data to a processing array, as a parallel output, said select portion depending upon the complex function.

- 16. The method of claim 15, wherein said processing array includes a plurality of adders.
- 17. The method of claim 15, further comprising:

  providing a twiddle factor as the operational factor, for performing discrete Fourier transforms (DFTs); and

selectively engaging at least a portion of the processing array, thereby controlling a data size processed by the processor array.

18. The method of claim 15, further comprising accumulating the data output from the processing array.